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MACC – Deucalion

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RCTS100
POAT 2020 Programa Operacional Assistência Técnica
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FUJITSU

Advanced computing research and innovation

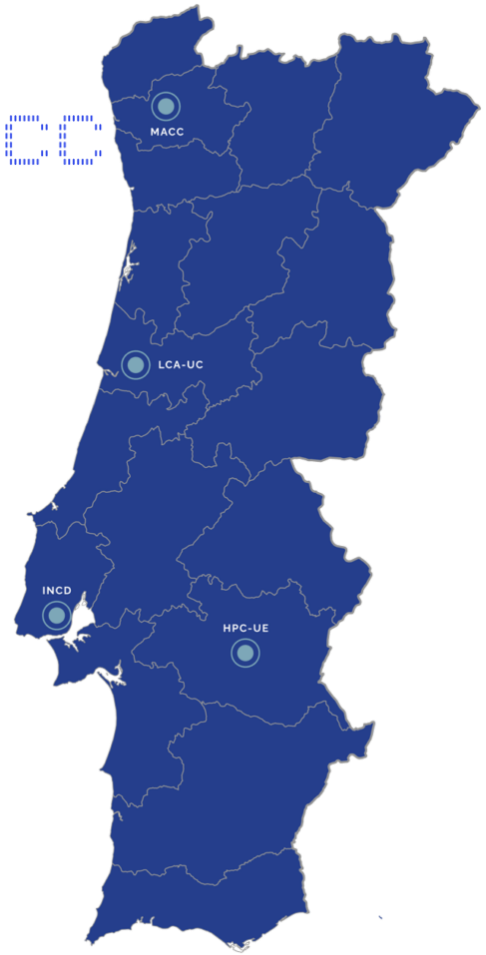
Support and foster research and innovation on the codesign of HPC systems from their implementation to optimization and exploitation, a major priority towards Europe's HPC and EPI initiatives.

Computational science and engineering, and Artificial intelligence research

Foster the creation, expansion and consolidation of research and innovation teams on national and European high priority scientific domains requiring large scale digital simulations and data intensive systems and applications.

Public services and enterprises

Offer of advanced computing resources and consultancy to science and higher education institutions, public administration, academic entrepreneurship and enterprises for the curation, management and processing of big data and machine learning workload.



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DEUCALION

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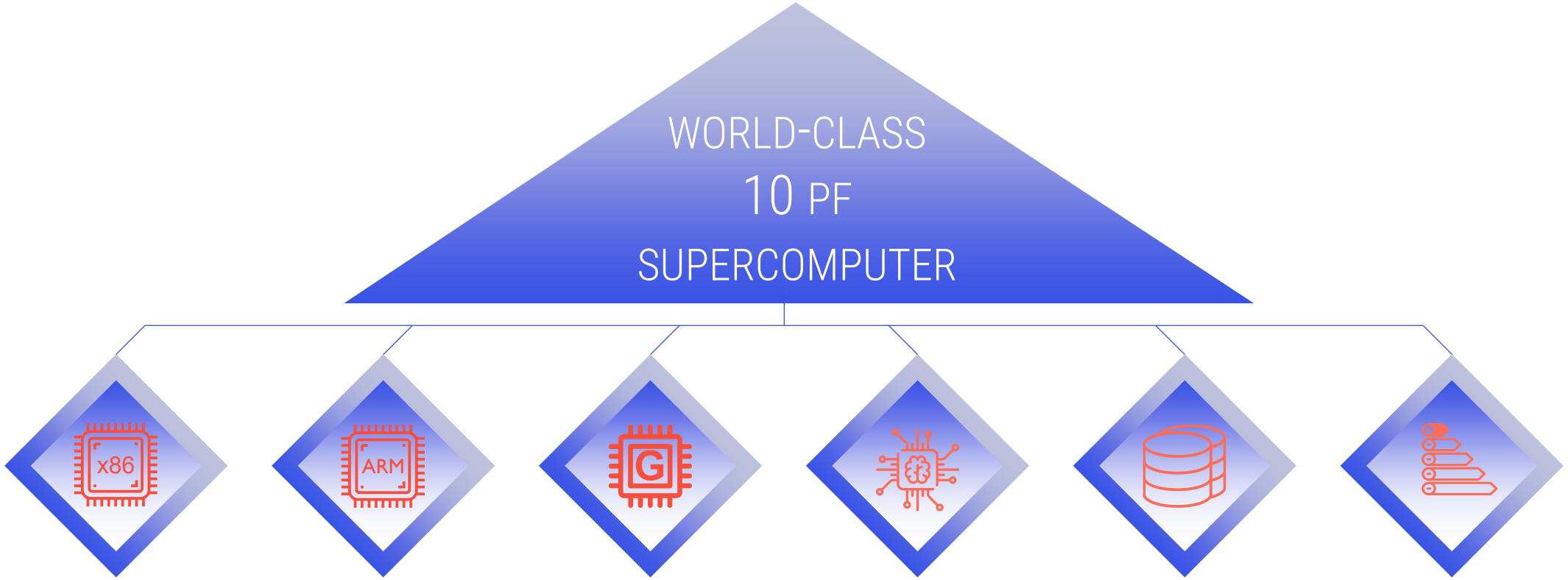

NEXT GENERATION X86 GENERAL PURPOSE SYSTEM AS THE POWERHOUSE FOR CONVENTIONAL DIGITAL SIMULATIONS

STATE-OF-THE-ART ARM GENERAL PURPOSE SYSTEM WITH THE SHORT-TERM OBJECTIVE OF BUILDING HPC SCIENCE AND ENGINEERING CAPACITY

GGPU ACCELERATORS ON 10% OF THE X86 SUBSYSTEM MAINLY DEVOTED TO DATA SCIENCE APPLICATIONS

EXPERIMENTAL TECHNOLOGIES TOWARDS INNOVATIVE ARCHITECTURES WITH POTENTIAL FOR EXASCALE

HIGH PERFORMANCE DEPENDABLE STORAGE SYSTEM WITH 10 PB NET CAPACITY

AMBITIOUS POWER USAGE EFFECTIVENESS (PUE) OF 1.1

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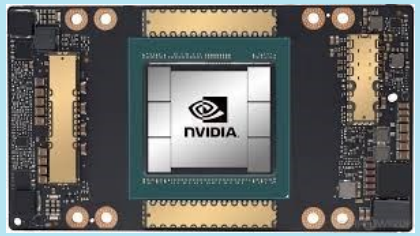
Deucalion Compute Nodes

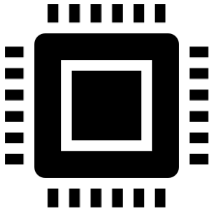
Compute nodes – 1632
Cores Number – 78,336
Memory Capacity – 52 TB
Rpeak – 5.013 PFlops

Compute nodes – 500
Cores Number – 64,000
Memory Capacity – 128 TB
Rpeak – 2.304 PFlops



Compute nodes – 33
CPU Cores Number – 4.224
Memory Capacity – 16 TB
GPU Memory – 8 TB
Rpeak CPU – 152,064 GFlops
Rpeak GPU – 2.572 PFlops

10 PFlops



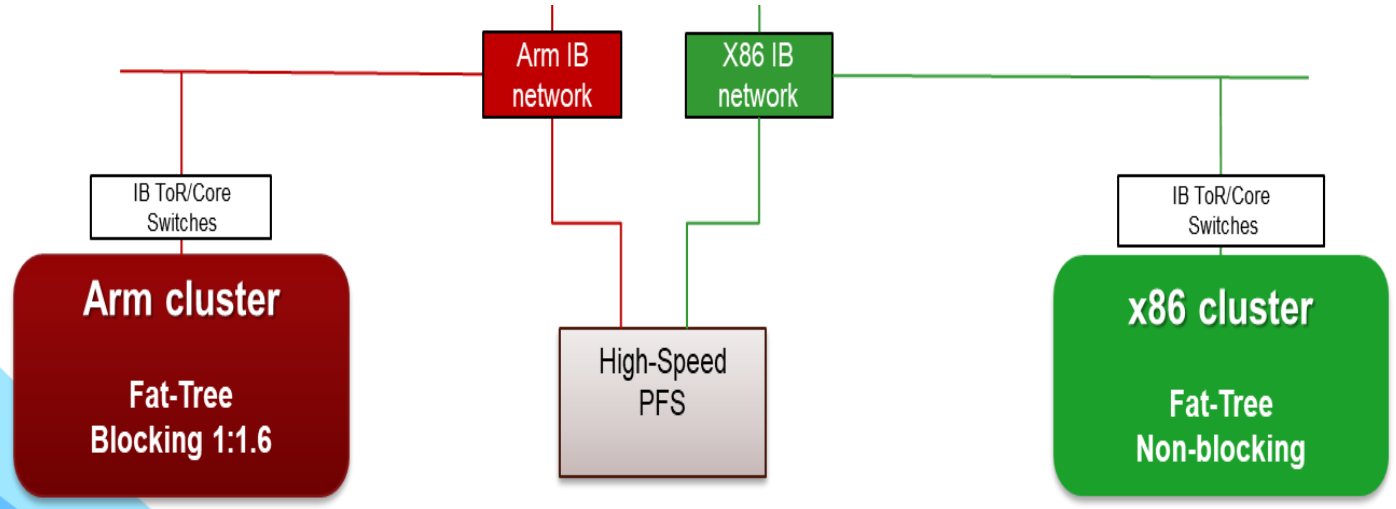
2 clusters / 3 partitions

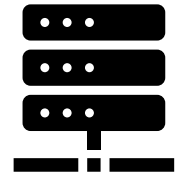
- The ARM cluster is based on the Fujitsu A64FX processor with high levels of performance with low energy consumption
- The x86 cluster with AMD EPYC highly efficient processor with very good HPL efficiency and excellent energy
- The accelerator nodes have Ampere GPU from NVIDIA

High Speed Interconnect

InfiniBand

ARM Compute Nodes – HDR100
X86 Compute Nodes – HDR100
X86 Accelerated Nodes – HDR200
I/O Nodes – HDR100
Other service Nodes – HDR100

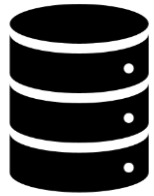




- Effective parallel execution and data processing on the cluster relies on an efficient and balanced high-speed interconnect.
- Both IB networks have 32 paths to storage enabling either cluster to exercise the full bandwidth to disk on its own.

Deucalion Storage

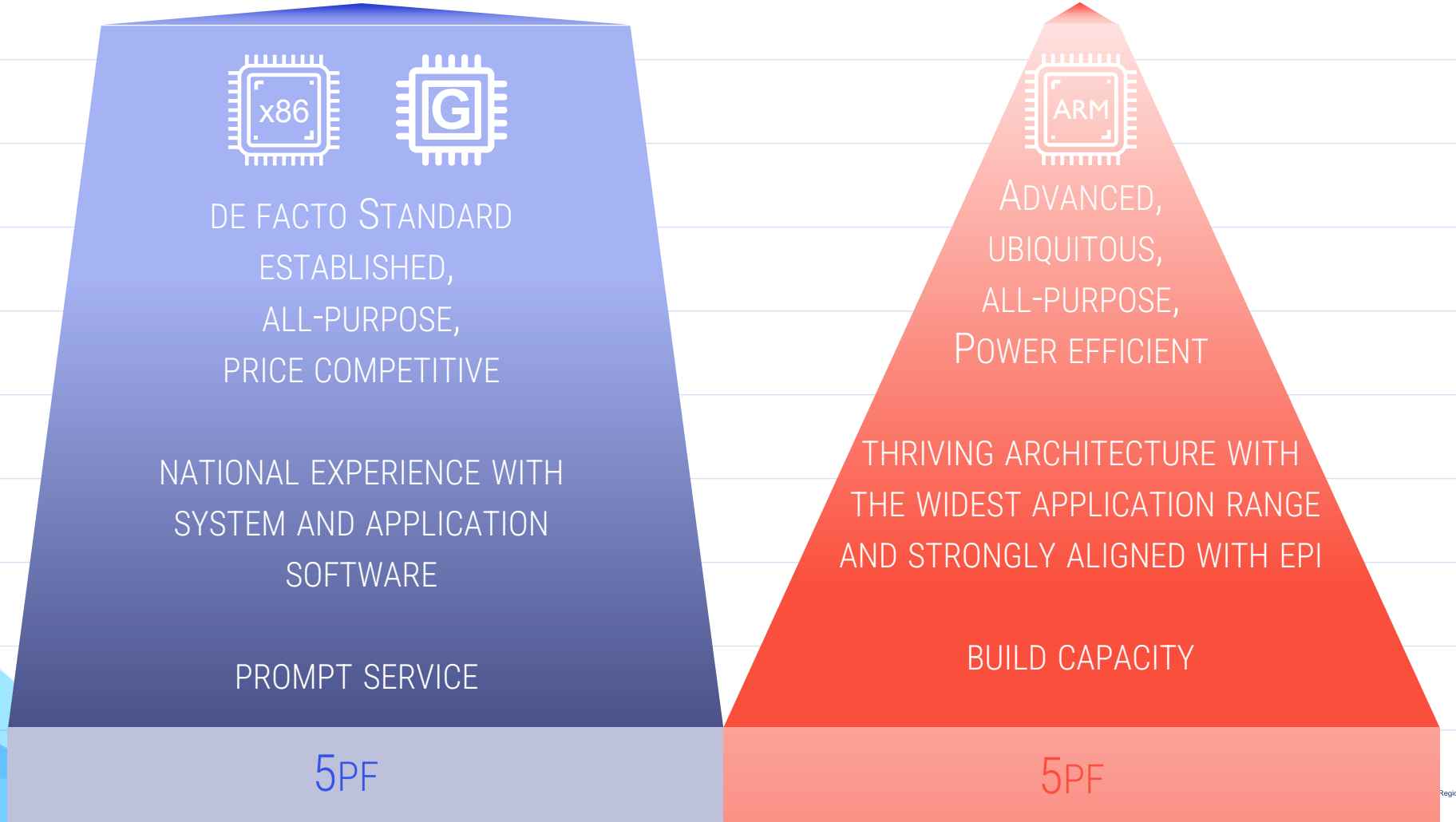
High Speed Storage	**Metadata and Hot Pools NVMe** – 430 TB usable **HDD Datapools** – 10 PB usable **MDS Servers –** 8 Nodes **OSS I/O Servers** – 32 Nodes **Filesystem** – Lustre PFS **Aggregated Performance** - 340GB/s in reads, 260GB/s in writes
NAS Storage	**Total SSD net Capacity** – 50 TB **Data Modules** – 2 for redundancy **Connection type –** 8x10 GbE



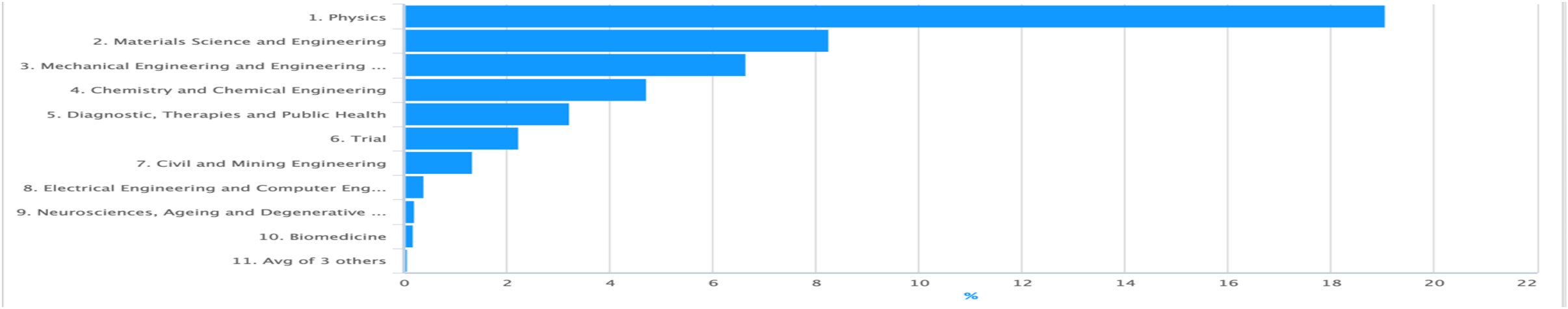
- Building block architecture High speed storage with both an NVME tier and a traditional PFS disk-based tier

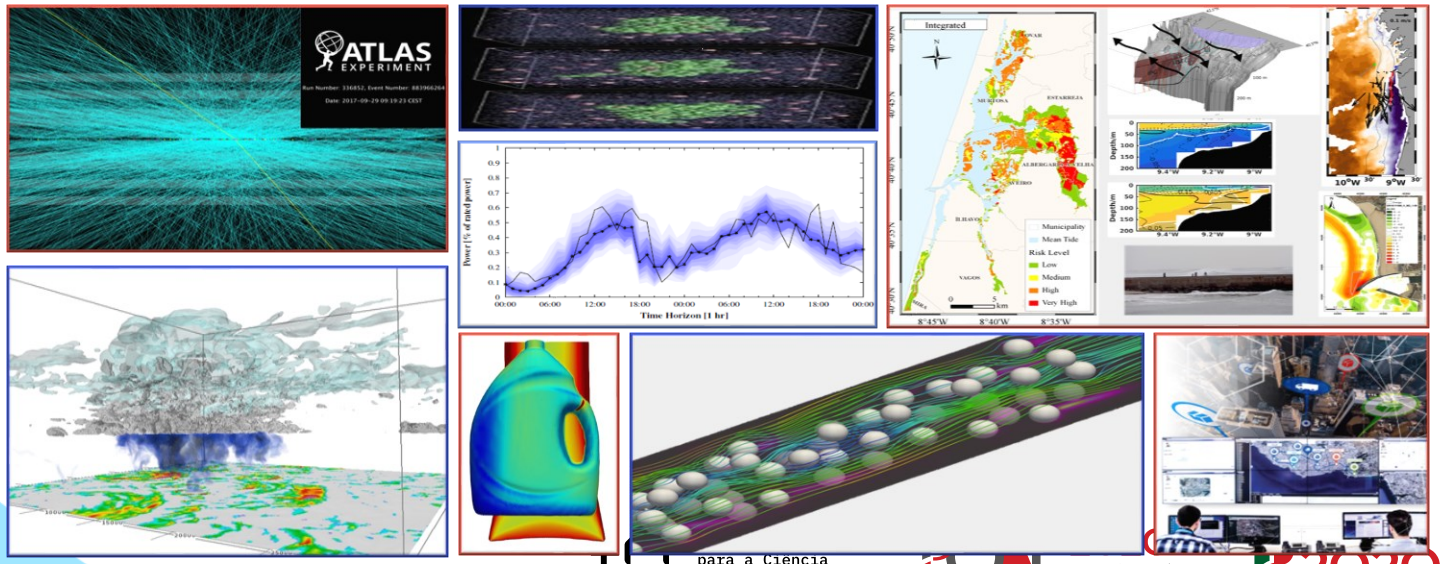
- NAS subsystem for the purposes of the user homes (/home), application sources and binaries (/apps), as well as Job Spool and node images. Provides visibility of data across all clusters and servers.

A HETEROGENEOUS ARCHITECTURE, AN OVERARCHING GOAL



Science to come…





Thank you for attending!

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