22 e 23
OUTUBRO

encontro de computação avançada 2025

Universidade de Aveiro,
Edificio da Reitoria

Parceiro: comudel

Apoios: AI Factory

EUROCC PORTUGAL

EuroHPC Joint Undertaking

Financiado pela União Europeia NextGenerationEU

Portugal@EuroHPC projects&consortia: from HPC to Quantum

Leonel Sousa, INESC-ID, Instituto Superior Técnico, Universidade de Lisba

FCCN | fct | CNCA | universidade de aveiro theoria poiesis praxis | Parceiro: comudel | Dias de Sousa INSTRUMENTAÇÃO ANALÍTICA E CIENTÍFICA, S.A. | Apoios: AI Factory | EUROCC PORTUGAL | EuroHPC Joint Undertaking | PRR Plano de Recuperação e Resiliência | REPÚBLICA PORTUGUESA | Financiado pela União Europeia NextGenerationEU

EPI

European Processor Initiative (SGA1, SGA2)

- **European independence in HPC processor technol.**

- Entering HPC market with:
  - **European server-class compute chips for the first time**
  - **European software environments and tools optimized for hybrid computing**

- **Single node is mainly targeted**

- **End-to-end security**

EuroHPC Joint Undertaking

January 2019- December 2025

SGA1 - 80 M€
SGA2 - 70 M€

Total - 150M€

IST @ EPI

- Accelerator co-design based on the Cache-Aware Roofline Model [1]
- Next-generation floating-point arithmetic unit architectures for AI/ML and HPC applications [2]
- RISC-V ecosystem advancement
  - Standard performance monitoring at user level [3]
  - New specifications for event-based sampling [4]
- EPI EPAC1.0/1.5 Test Chips Testing and Evaluation

[1] A. Ilic et al., "Cache-aware Roofline Model: Upgrading the Loft", IEEE CAL, 2014
[2] L. Crespo et al., "Unified Posit/IEEE-754 Vector MAC Unit for Transprecision Computing", IEEE TCAS-II, 2022
[3] J. Domingos, et al. "Supporting RISC-V Performance Counters through Linux Performance Analysis Tools." ASAP 2023
*[4] T. Rocha et al. "RVEBS: Event-Based Sampling on RISC-V", DATE 2025 (**best paper award candidate**)*

Digital Autonomy for RISC-V in Europe

Main objectives:

- **Boost Europe's digital autonomy** in HPC and AI through fully European, RISC-V–based hardware and software solutions.
- **Set a roadmap for post-exascale European supercomputers, laying the** foundation for next-generation HPC systems.
- **Develop three advanced chiplets** (vector, AI, and GPP) and an optimized software stack using a co-design approach.

SGA1: March 2025 – February 2028 240 M€

dare (SGA1)

Portuguese involvement and contributions:

- **Task 18.7 GPP-specific SW Tools**, to optimise the GPP applications and provide load-balancing. **[Task Leader]**

inesc id lisboa Cache-aware Roofline Model (CARM) framework and supporting tools.

- **Task 27.1 Node services**, to provide a complete SW stack for cutting-edge HPC and AI applications, optimised for the DARE hardware:

inesc id lisboa Online lightweight performance measurement tools – PAPI and event-based sampling (EBS).

- **Task 27.2 Compilers**, complete SW stack for the DARE hardware:

INESCTEC Prototype advanced transformations using source-to-source infrastructure.

POP3

Performance Optimisation and Productivity 3

- **Centre of Excellence in HPC**

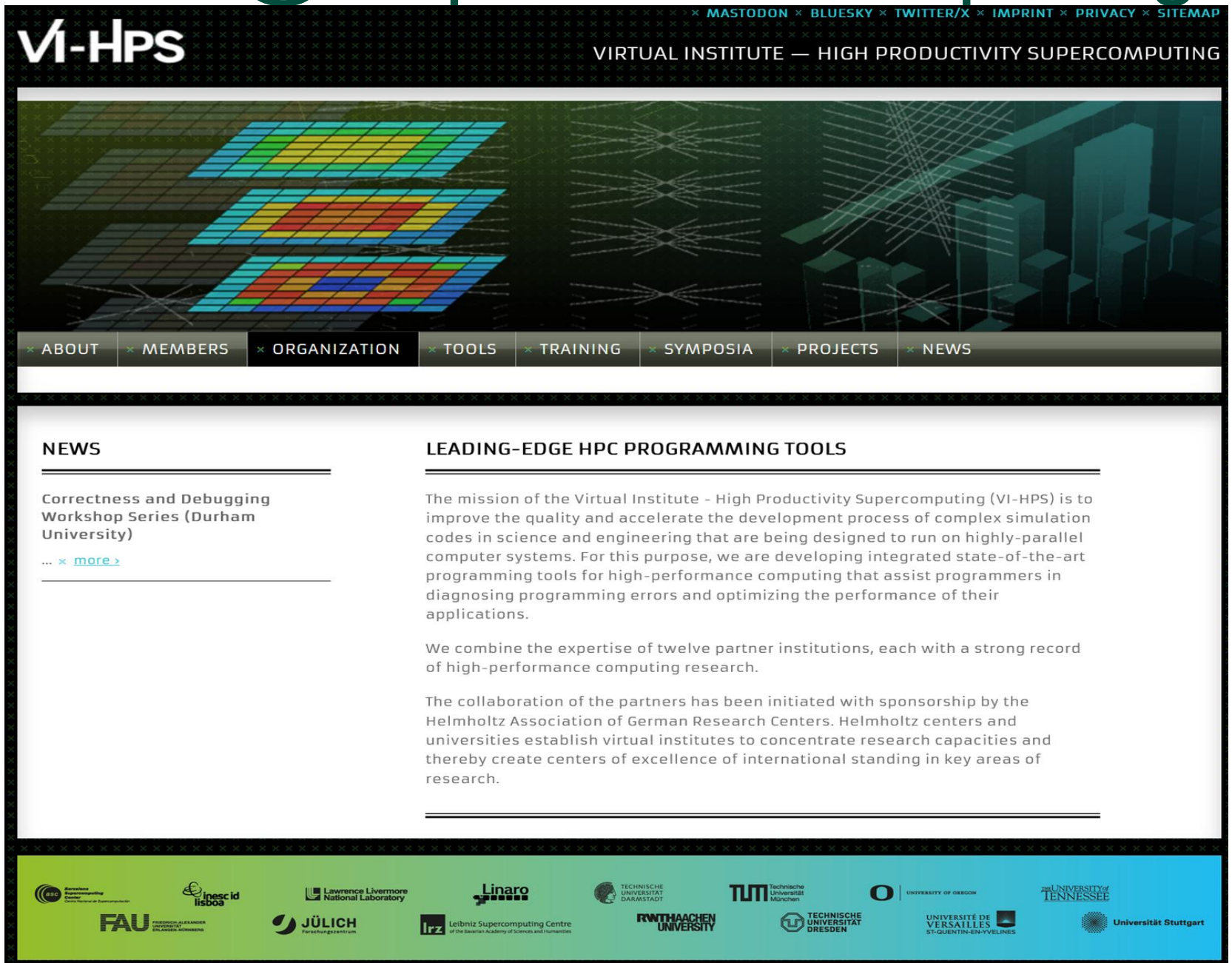
- Provides services to users and developers of HPC applications
  - **Primary service** to identify performance issues and suggest best practices
  - **Second level services** proof-of-concept, correctness-check, energy-efficiency study

- **Provides training on the methodology**
  - Webinars and dissemination also via participation in HPC conferences and workshops

January 2024 - December 2027

€5 996 896

INESC-ID @ https://www.vi-hps.org/



INESC-ID @ POP3

- Multidisciplinary team with know-how in HPC programming and tools
- Performance assessments of different types of applications (5 now)
  - Targeting different CPUs/GPUs with different programming models
  - Relying on POP methodology using tools from the project partners
- Development of tools and models for assisting with the assessments
  - Cache-Aware Roofline Modeling (CARM) Tool [1]
  - Integration with the Paraver performance analysis tool https://pop-coe.eu/blog/tool-time-carm-paraver-integration
- Publications on state-of-the-art codes targeting supercomputers [2,3]

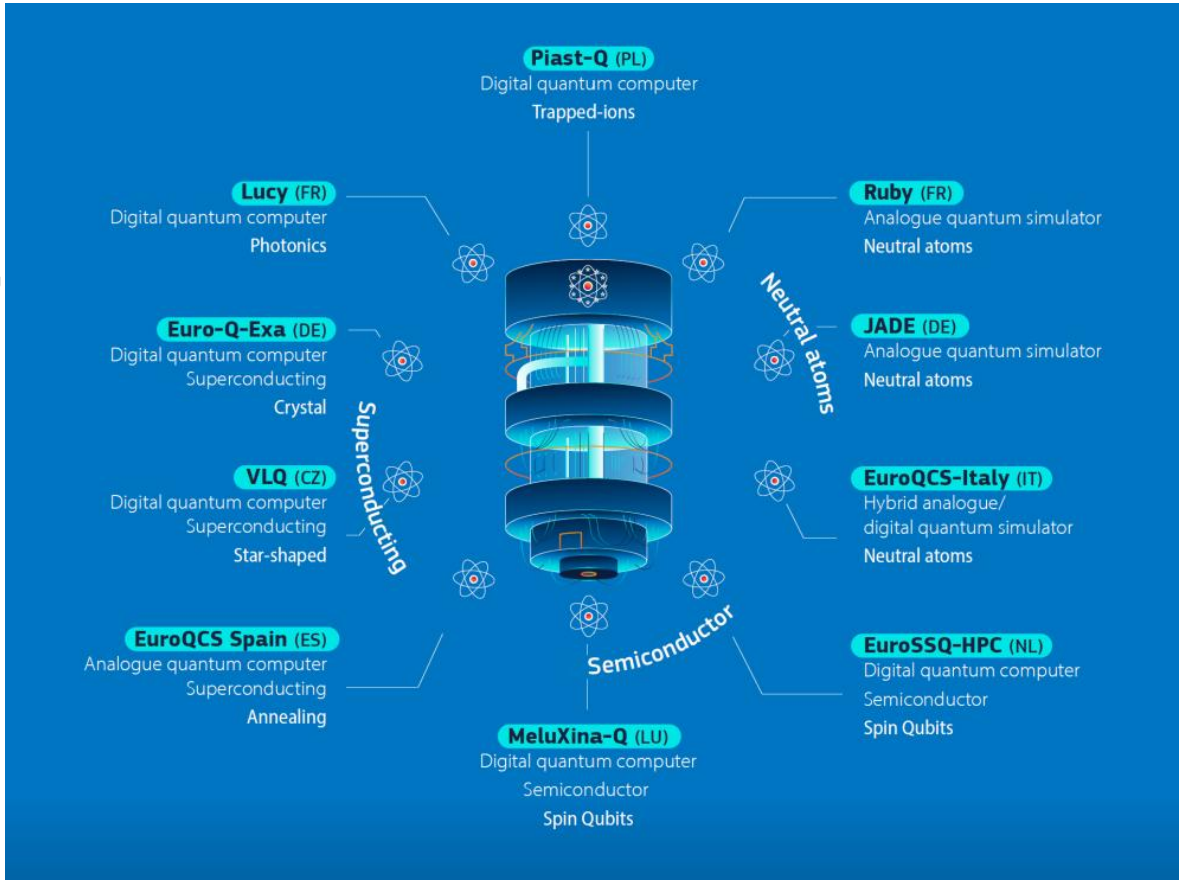
[1] J. Morgado, L. Sousa, A. Ilic, CARM Tool: Cache-Aware Roofline Model Automatic Benchmarking and Application Analysis, IEEE IISW'24
[2] R. Nobre et al., EPIClear: Exploiting Domain-Specific Features for Epistasis Detection Acceleration on Tensor Cores, ACM ICS '25
[3] R. Nobre et al., Porting Epistasis Detection Methods to EuroHPC Supercomputers, Procedia Computer Science, 2025, Elsevier

Quantum Computing EuroHPC

- **I am teaching the basics of QC to ECE and CSE MSc students [1]**

- **QC is still quite immature at the technological and system levels**
  - Analogue *vs* Digital, 10-140 data qubits!
  - Reduced set of developed algorithms (QFT, Shor, Grover,…) .
  - Neither tools nor frameworks for programming at a high level!

- **At a first stage, they can be Domain Accelerators at HPC Centres**
  - I was invited for a quantum computing COST Action project proposal.



[1] L. Sousa, Crash Course on Quantum Computing for Engineering Students, IEEE IPDPSW'25

Thank you.

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Obrigado.

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